



S/N 10/081818

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Jerome M. Eldridge et al. Examiner: Tu-Tu Ho
Serial No.: 10/081818 Group Art Unit: 2818
Filed: February 20, 2002 Docket: 1303.045US1
Title: ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW ASYMMETRICAL TUNNEL BARRIER INTERPOLY INSULATORS

COMMUNICATION CONCERNING RELATED APPLICATION(S)

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Commissioner for Patents
P.O. Box 1450
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Applicants would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

<u>Serial/Patent No.</u>	<u>Filing Date</u>	<u>Attorney Docket</u>	<u>Title</u>
09/945507	August 30, 2001	1303.014US1	FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945395	August 30, 2001	1303.019US1	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/943134	August 30, 2001	1303.020US1	PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS
09/945498	August 30, 2001	1303.024US1	INTEGRATED CIRCUIT MEMORY DEVICE AND METHOD
09/945512	August 30, 2001	1303.027US1	IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS

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09/945554	August 30, 2001	1303.028US1	SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945500	August 30, 2001	1303.029US1	PROGRAMMABLE MEMORY ADDRESS AND DECODE CIRCUITS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/028001	December 20, 2001	1303.035US1	PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL BARRIERS
10/177096	June 21, 2002	1303.063US1	GRADED COMPOSITION METAL OXIDE TUNNEL BARRIER INTERPOLY INSULATORS
10/789038	February 27, 2004	1303.024US2	INTEGRATED CIRCUIT MEMORY DEVICE AND METHOD
10/783695	February 20, 2004	1303.019US2	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/781035	February 18, 2004	1303.063US2	GRADED COMPOSITION METAL OXIDE TUNNEL BARRIER INTERPOLY INSULATORS
10/788810	February 27, 2004	1303.027US2	IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/819550	April 7, 2004	1303.019US3	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS

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Respectfully submitted,

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By


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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 13th day of May, 2004.

Name

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